Trace Recording with the LPC2000 Microcontroller Family

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The Embedded Trace Macrocell (ETM)

In addition to the standard debug features of ARM cores, ARM offers the opportunity to add the ETM core into ARM implementations. The ETM gives the chance to trace program flow with an external debug tool, thus making the application development more efficient and straight forward. From the microcontroller vendor's viewpoint, the ETM makes the chip more expensive due to the additional logic and pins required. To find the best compromise between cost and debugging benefit, the ETM can be included in different configurations: small, medium and large. The small mode has the least number of ETM features included and the smallest silicon size. The large mode has the highest silicon costs but also the greatest ability to extract trace data, filter and control the trace recording.

Unlike most other general purpose ARM7 microcontrollers, the Philips LPC2000 family has the advantage of an included small-mode ETM. The ETM is able to deliver information about executed branches, data accesses and the state of instruction execution. This information has to be collected in an external trace buffer and interpreted and displayed in a convenient and readable form.

Trace with TantoPT-ARM and HiTOP

In conjunction with Tanto-PT, HiTOP reads out, interprets and displays the recorded trace data. The display can be performed as raw trace, as instruction trace and in high-level language lines mode (HLL). For trace interpretation, the branch messages are completed with the intervening instructions. This is done automatically from the code information of the loaded application.

In the raw trace window, the bus cycles are reconstructed - the columns "Address" and "Data" are self-explanatory. The "State" column shows the status of the cycle and the "Add.Stat" column shows detailed descriptions of the instruction execution, described in more detail in the ETM Specification by ARM.

Abbreviation	Meaning
IE	**Instruction executed**
ID	**Instruction executed with data**
IN	**Instruction not executed**
BE	**Branch executed**
BD	**Branch executed with data**
WT	**Wait (no cycle executed)**
TD	**Trace disabled**
TR	**Trigger**
OF	**Overflow**

Table 1 Bus cycle states displayed in the Trace window

In the instruction trace window, all cycles corresponding to an instruction are collected and displayed as opcodes in mnemonics. Related data accesses are displayed after the instruction.

The "State" column shows additional states with the following abbreviations: **BRAD**, **O**, **R** or **W**. **R** and **W** denote read or write cycles, **BRAD** denotes branch address, an artificial state derived from the branch message of the ETM. **O** means an overflow of the internal ETM FIFO.

The "Lines" display shows the reconstructed HLL lines from the ETM information.

The desired trace display mode (Instruction, Raw, Lines) can be switched via the trace window's context menu.

Controlling and Filtering the Trace Recording

To optimize trace recording and the trace window, some settings are necessary:

1. **General Settings ("Project Settings" dialog box, "Emulator Settings >Trace Setup" item)**

   The trace buffer can be cleared with each emulation start or it can be appended to the previous recording with the setting “Buffer on start”.

   The trace buffer can be frozen when full or it can be overwritten as a wrap-around buffer using the setting “Action on buffer overflow”.

   The listing can be started from the newest or the oldest frame (“Display mode” setting).

2. **ETM-Specific Setting ("Project Settings" dialog box, "Target Settings > ETM Configuration" item)**

   The "ETM port size" and "ETM port mode" has to be set according to the ETM of the LPC2000. The ETM size is “small” and the mode can be selected as normal or half-rate clock. In normal clock mode, the trace data is sampled at each rising edge of the clock and in half-rate clock mode, the trace data is sampled at each rising and falling edge of the clock. The trace clock is half of the ARM clock.

   If the "Cycle accurate tracing" setting is enabled, all trace data including **TD** cycles are recorded.

   The "FIFO warning level" determines how full the internal ETM FIFO must be for an overflow message to be displayed. It is recommended to select 100%.

   The recording of coprocessor cycles can be switched on or off ("Monitor coprocessor cycles").

   With the "Trigger Delay Counter" setting, the proportion of the trace buffer before and after the trigger event can be chosen. The trigger event is described in section 3 (see below).

   For the "Data tracing", it is important to prevent ETM FIFO overflows and to select the filtering options carefully. If you only want to record the program flow of the application, the "data tracing disabled" option is recommended. In this case, only the branch messages are transmitted from the ETM and no ETM FIFO overflow will occur. With this setting, no data accesses will be recorded. If you want to see the values which are written or read from/to a variable, you will have to select "both address and data". In this case the information flow increases and it is very likely that an ETM FIFO overflow will occur. You can avoid this by filtering the trace, as described in section 3 (see below). With the options "only address portion" or "only data portion", the selected data information is passed to the Tanto-PT and will be displayed in the Trace window. These selections may be meaningful in conjunction with trace filtering.

3. **Controlling and Filtering the Trace (Trace window's context menu: "Filter" command, Trace control window's context menu: "Change" command, Trace Trigger dialog)**

   Trace recording can be enabled, disabled, triggered and filtered with the ETM logic and is controlled by means of the Trace window's context menu having the “Filter…” command selected.

   Click on the “Advanced” button to have access to all dialog features. The trigger or filter event is defined by an address or address range, an optional external input and the bus state. The option field "Trigger Type" is overwritten by the bus state and the value range is not recognized.

   For the address condition there are several selections possible: an address with don’t-care address bits, a single address or an address range. Don’t-care bits are marked with an ‘X’ (please refer to the HiTOP online help for more information on address inputs). The bus state can be: "Execute", "Read", "Write" or “Read/ Write”. In addition, the "Fetch" state is possible, meaning that the instruction was fetched but not executed. Since all ARM instructions can be conditional ones, also the states "CondPass" (condition passed) and "CondFail" (condition failed) are available.

   The "External Input" field can be used if external signals are connected to the data probe of the Tanto-PT.

   The "Action on Trigger" field defines the action which is executed when the specified trigger condition is true.

   The "Enable" and "Disable" options switch the trace recording on or off. The "IFltInc" or "IFltExc" options allow the recording of instructions with the specified trigger condition or the exclusion of them and the recording of all other instructions. With the "DFltInc" or "DFltExc" options, data accesses defined in the trigger condition can be included or excluded from recording. Please note that with these data filters those instructions are also included in the trace that are responsible for this data access.

   The "Trigger" option enables the trace with the trigger position defined in section 2 (see above). There is only one trigger possible.

   With the "Enable", "Disable" and "Trigger" options no address ranges are possible.

   The small mode ETM of the LPC2000 microcontrollers has limited trigger resources which allow only one event definition with an address range or two events with single addresses.