

JTAG Debugger
Trace Emulator
Code Coverage Module

Solutions & Tool Chain for XC166 for Controllers based on the C166S V2 Core



Embedding Software Quality



The C166S V2 Core from Infineon

The OCDS Debug Solution: TantinoXC

Derivates based on the C166V2 core come complete with an OCDS (On Chip Debug System) debug interface. This interface facilitates debugging based on a JTAG connection to a target system.

With the TantinoXC debug tool, Hitex is presenting a high-performance OCDS Level 1 JTAG debug solution for the XC166 family from Infineon Technologies. The device is USB powered and connected.

TantinoXC supports all OCDS features. The sophisticated hardware design is the basis for the outstanding performance. In addition, special features, such as support of interrupts during halted emulation, facilitate the debugging work. Through automatic target voltage adjustment, safe operation is guaranteed between 1.3 and 3.3 V.

Internal and external FLASH modules are programmable with TantinoXC.

Entry-level Solution: TantinoXC



The Emulation Device

To provide debugging beyond the possibilities of the OCDS (On Chip Debug System) interface of the standard XC166 devices, Infineon developed the Emulation Device. This dedicated chip consists of a standard device combined with a special emulation carrier chip. Based on the Emulation Device (ED) high-end debugging with features like Flash memory replacement, trace recording and sophisticated trigger events is possible.

Target Connection

For OCDS debugging a JTAG connector should be available on the target hardware. However, if a JTAG-connector is not available, Hitex offers a direct adaptation to the chip using its patented PressOn technology. This avoids the need for additional space to accommodate a JTAG-connector on the PCB - which could be useful for the debugging of production units.

From OCDS to Advanced Debugging

The DProbeXC

The DProbeXC incorporates the ED-chip and makes all of its advanced debugging capabilities available to the user. Features like Flash memory replacement, where an on-chip RAM is used instead of the Flash memory (of course with the same timing) simplify and accelerate debugging of single-chip applications. Of course the DProbeXC also allows the programming of the on-chip Flash of the target CPU without the need of an additional tool. Other functions, like the Fast-Break, allow access to the on-chip peripherals, registers and memory in real-time, thus enabling the test and calibration of the "living" application. For more extraordinary features of the DProbeXC, see table on the last page.



DProbeXC

The DTraceXC

The DTraceXC extension module enhances the DProbeXC with trace recording capabilities. Its 128 k frames trace memory records all important status information to analyze the program flow. Using its qualified trace recording capabilities, the DTraceXC allows selective evaluation of specific software modules or tasks. Time measurements with 12.5 ns resolution allows the user to identify the bottlenecks in his application and are the best start for your optimization process. Chip external signals may be analyzed using the optional data probe which connects to the trace module.

Target and Host Connection

In order to establish a reliable link to the target system, Hitex provides various adaptation solutions, e.g. the PressOn adapters. The DProbeXC uses the Hitex proprietary HIF interface for host communications. The user may choose between a PCI card, a PC-Card (PCMCIA) or a LPT connection.

Code Coverage with DCoverageXC

DCoverageXC – Module For Code Coverage

The coverage module plugs onto the DProbeXC. On its top side an optional DTraceXC can be added.

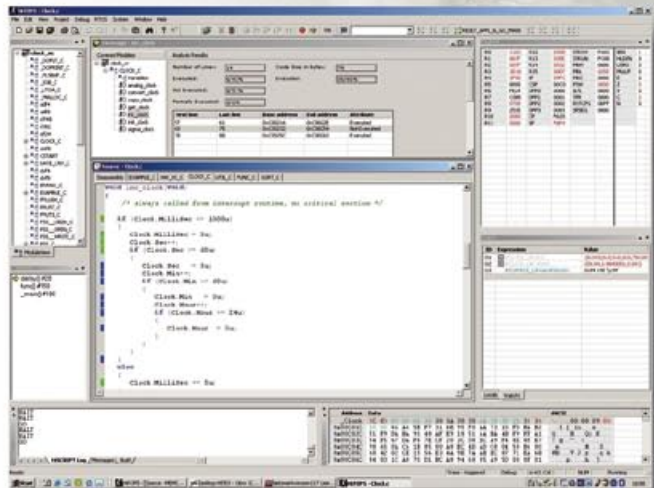
Recording and Reading of Information

The hardware provides 16 coverage ranges (128k/each) for the registration of read/write-accesses. Each of these ranges can be used for the registration of code or data accesses. Recording of code and data coverage is possible simultaneously within the same range.

Address accesses covered by a data coverage range are recorded in a byte-accurate manner as read/write-accesses. This enables the user to record a memory range of 2 MB maximum by using the coverage analysis. The coverage information can be read without interrupting the recording. Whether external or chip-internal memory is available, the user can check all accesses within the controller's entire address range.

Functionality Software

HiTOP identifies the code range during loading and automatically sets up the regions with these initial values.



Code coverage as line attribute

- > Visualization in the source window as a coloured line attribute with the values “not executed”, “partly executed” or “executed”
- > Visualization in the Disassembly window as a coloured line “not executed”, “executed”

Code coverage in a separate window

Visualization of selectable modules/functions/lines in a separate coverage window – relative coverage in percent and absolute display of lines (from - to). The referring ranges can be selected from the work space by drag&drop or by indicating the range.

The Operating Environments

HiTOP Debugger

Our proprietary user interface HiTOP supports very sophisticated HLL-Debugging and allows an easy transition between different types of tools and CPU platforms. The HiTOP debugger offers software and hardware breakpoints and implements fast-breaks for on-the-fly access to any memory and internal register. The on-chip Flash memory is fully supported by HiTOP and can directly be programmed using user-friendly commands.

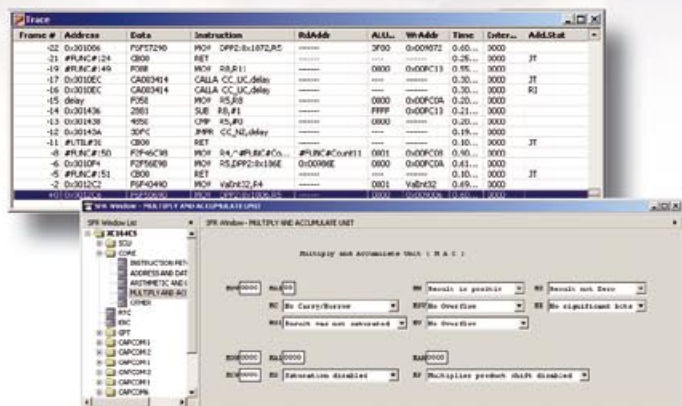
The Operating Environments

HiTOP supports all leading compilers and their object formats. Many third-party tools are well integrated with HiTOP because of the acceptance of HiTOP as standard emulation control software. HiTOP also supports all major embedded real-time operating systems, giving a fully transparent overview of your whole software system at any time by displaying information such as task lists, the status of a specific task, message queues, delays and memory objects.

Data coverage

HiTOP identifies the data range during loading and defines this as default data coverage region. Data coverage is visualized in the memory window as a coloured attribute for each memory object. The display type BYTE shows the attributes “written”, “read”, and “written and read” in a coloured way. If the object contains different attributes, the attribute “mixed” will be displayed.

In the watch/quickwatch window data coverage is visualized as a coloured attribute for the referring symbol in the symbol column. Here no coverage attributes are provided to the value displayed. Instead only value changes are highlighted here.



The Basic DProbeXC Emulator

Supported Processors	XC161CJ, XC164CS, XC167CI and future XC16x derivatives
Emulation processor	Emulation device, fully transparent, non-intrusive debugging
Operating voltage	Supports voltages from 2.7 up to 5.5 Volts
Overlay memory	1 MByte mapable in complete 16 MByte address range Selectable granularity (1 kByte up to 32 kByte) Zero wait state access Write protection (ROM emulation)
On-chip ROM	Selectable ROM size up to 512kByte
Breakpoints	32 hardware execution breakpoints (break before make) 256 software breakpoints, On-the-fly accesses to registers, internal and external RAM and Flash memory
Clock generator	Programmable clock generator (XTAL1) XTAL3-support integrated on DProbeXC
Control lines	Enable/disable control for RESETIN, RESETOUT, NMI, XTAL2
Adaptation	Adaptation via quad connector system to all existing adapter and chip packages. Compatible with Hitex PressOn technology
Connection to host	HIF PCI card, HIF PC card (PCMCIA), LPTHIF (Printer Port) Download rate up to 300 kByte/sec
Power	Individual power supply (80-260 VAC) or direct 5V DC connection
Approvals	CE, GS, FCC, UL, CSA

DTraceXC

Trace memory	128k frames trace memory (192 channels)
Timestamp	12,5 ns resolution
Events	4 complex events
Event actions	Break, trigger, qualify trace, start/stop trace, change level
Sequence levels	4 sequencer levels
Break sources	Single event, ORed event, End of recording
External lines	8 configurable, 110 channels

DCoverageXC

RAM download	200 kByte/sec
FLASH download	40 kByte/sec
Connection to target	16-pin, 2.54 or 1.27 mm interface
Special features	Support of interrupts during halted emulation; Break in Idle/Powerdown mod is possible; Automatic JTAG frequency control
FLASH Programming	yes
USB powered	yes
Host connection	USB full speed



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