

Product Information	<i>JProbeXC / DProbeXC</i>
Derivative	<i>Target Interface Description</i>
Version	<i>Infineon XC161/XC164</i>
Date	<i>1.0</i>
	<i>09. April 2002</i>

1. Preface

This application note is an information on the necessary debug interface to be implemented on XC166-based target systems. The information contained herein is specifically adapted to interface with the following emulation tools from Hitex:

- **JProbeXC (JProbe 200 hardware)**

The JProbeXC is the entry level tool for debugging XC166 based target systems. It provides all basic debug features like breakpoints, memory access or single stepping. The system uses the soldered-in target device (XC164CS or XC161CJ) for debugging. The interface to the target systems is performed by either a dedicated debug connector or via PressOn adapter.

- **DProbeXC**

The DProbeXC is the high-end debugging tool for the XC166 based target systems. Emulation is performed with a dedicated emulation device, which replaces the soldered-in target device. The system provides basic debug features as well as enhanced features like program flow tracing or performance measurements.

For further information please contact the Hitex Support Group at ++49-721-9628-0 or via Email at <mailto:support@hitex.de>.

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3. Debug Interface for JProbeXC

The JProbe200 is connected to the target system via a flat ribbon cable with female plugs and is connected to male headers on the JProbe and on the target. The OCDS1 connector defined by Infineon is a 16-pin standard 0.1 inch header (2 rows, 8 pins Type A). A 20-pin 0.05 inch SMD header (Samtec FTSH type) is also provided on the JProbe and requires less space (Type B); it is available with a keying shroud (FTSH-110-01-L-DV-K).

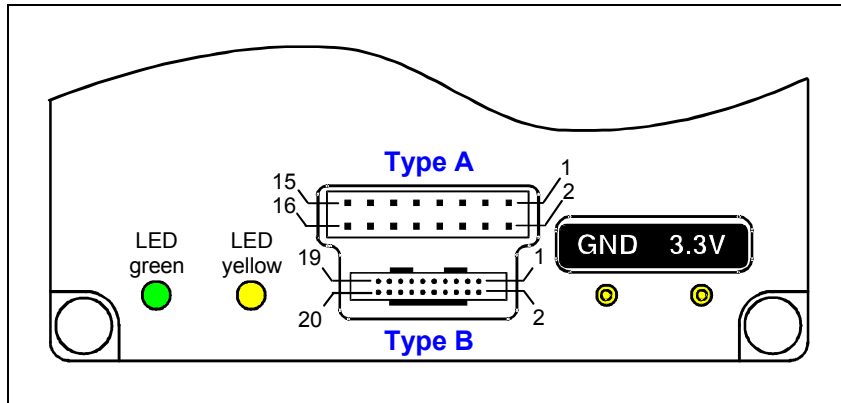


Figure 3-1: JProbe200 (Top View) - Location Of OCDS1 Connectors

3.1 Description of OCDS Level 1 Connector (Type A)

The following table shows the pin assignment and the signal description when using the 'Type A' interface (*Standard 0.1-Inch Header*).

Info	Signal ¹	Pin	Dir ²	Dir	Pin	Signal	Info
IEEE 1149.1	TMS	1	I	-	2	VCC	Power Supply
IEEE 1149.1	TDO	3	O	-	4	GND	Ground
CPU Clock (optional)	CPU_CLK	5	O	-	6	GND	Ground
IEEE 1149.1	TDI	7	I	I	8	RESET#	CPU's RSTIN# (open-drain)
IEEE 1149.1	TRST#	9	I	O	10	BRK_OUT#	CPU's BRK_OUT# signal
IEEE 1149.1	TCLK	11	I	-	12	GND	Ground
CPU's BRK_IN# signal	BRK_IN#	13	I	I	14	OCDS_E#	CPU's OCDS_E# signal
Not connected	NC	15	-	-	16	GND	Should be NO pin on the target (mechanical key)

Table 3-1: Signal Description of the OCDS1 Connector Type A

Note: For a detailed description and requirements of the IEEE1149.1 signals, please refer to the document '*JTAG-Connector & Device Driver Version 2.0*' from Infineon Technologies.

¹ Note: A '#' at the end of a signal name characterizes a low active signal

² Note: The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

3.2 Description of OCDS Level 1 Connector (Type B)

The following table shows the pin assignment and the signal description when using the 'Type B' interface (*Samtec 0.05-Inch Header*).

Info	Signal ¹	Pin	Dir ²	Dir	Pin	Signal	Info
Ground	GND	1	-	-	2	GND	Ground
IEEE 1149.1	TMS	3	I	-	4	VCC	Power Supply
IEEE 1149.1	TDO	5	O	-	6	GND	Ground
CPU Clock (optional)	CPU_CLK	7	O	-	8	GND	Ground
IEEE 1149.1	TDI	9	I	I	10	RESET#	CPU's RSTIN# (open-drain)
IEEE 1149.1	TRST#	11	I	O	12	BRK_OUT#	CPU's BRK_OUT# signal
IEEE 1149.1	TCLK	13	I	-	14	GND	Ground
CPU's BRK_IN# signal	BRK_IN#	15	I	I	16	OCDS_E#	CPU's OCDS_E# signal
Not connected	NC	17	-	-	18	GND	Ground
Ground	GND	19	-	-	20	GND	Ground

Table 3-2: Signal Description of the OCDS1 Connector Type B

Note: For a detailed description and requirements of the IEEE1149.1 signals, please refer to the document '*JTAG-Connector & Device Driver Version 2.0*' from Infineon Technologies.

¹ **Note:** A '#' at the end of a signal name characterizes a low active signal

² **Note:** The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

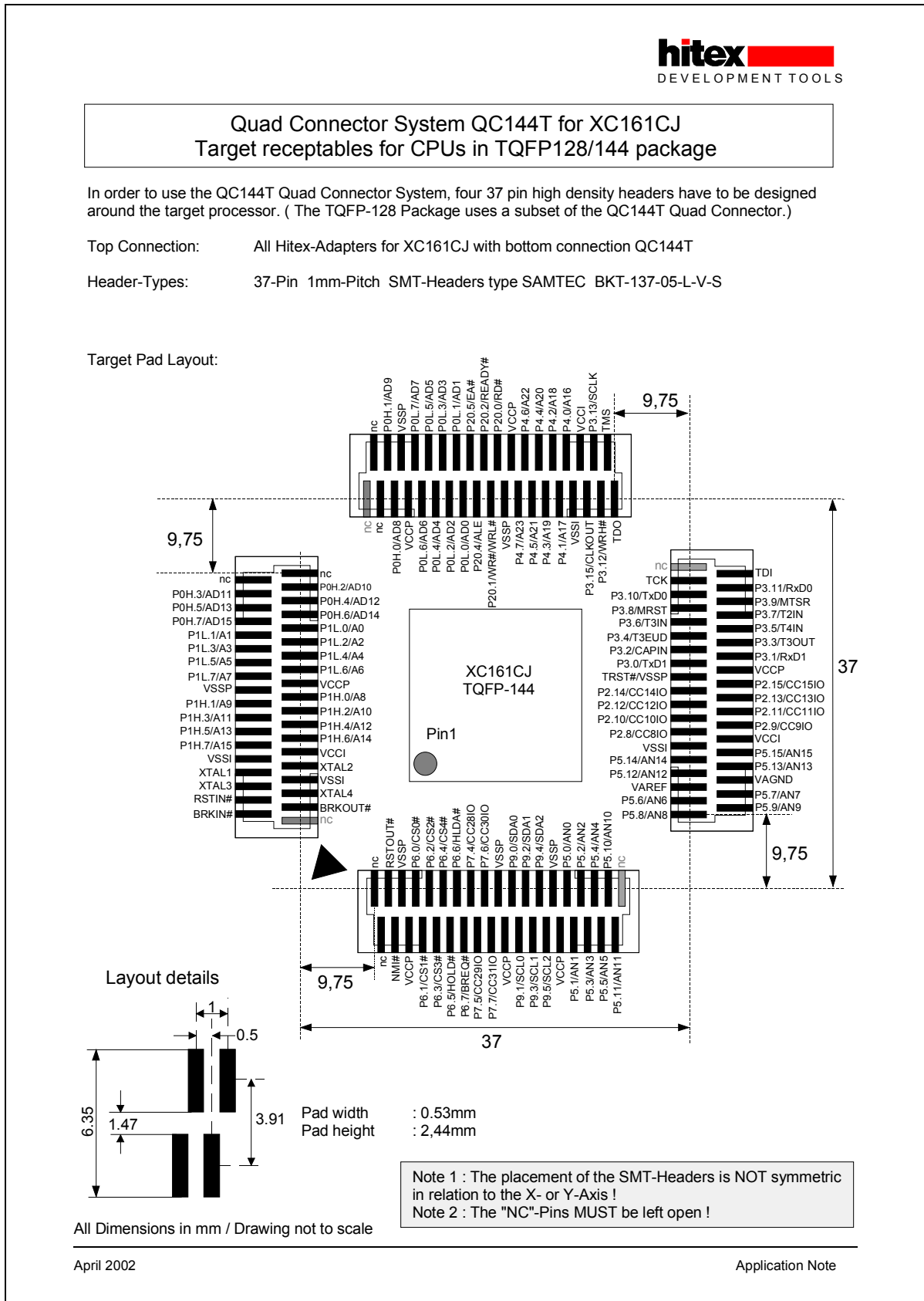
4. Target Interface for DProbeXC

Several options are available to adapt with the DProbeXC to a target system. Depending on the application's possibilities especially with regards to layout space requirements, one or more of the following adaptation solutions provide an effective solution:

- **Quad Connector**
The target system provides access to all CPU signals by implementing a quad connector interface on the application itself. This solution requires additional space on the target system itself and is in most cases only applicable for engineering or test boards. However, this solution is the most effective in terms of contact robustness and pricing.
- **PressOn**
The PressOn adaptation solution adapts on top of the original soldered-in CPU. There is only a minimum of board space requirement. The solution allows especially adaptation on production units, that do not have specific precautions for debugging.
- **Yamaichi**
The Yamaichi adapter allows to either use a standard CPU in the equivalent Yamaichi socket or to adapt the emulator on top of the Yamaichi socket. This solution is especially efficient when different device versions or ROM versions have to be verified in a target system.
- **Replacement**
The replacement adapter is soldered directly into the target system instead of the CPU.

4.1 Adapter Solutions for XC161CJ in TQFP144

4.1.1 Quad Connector Layout

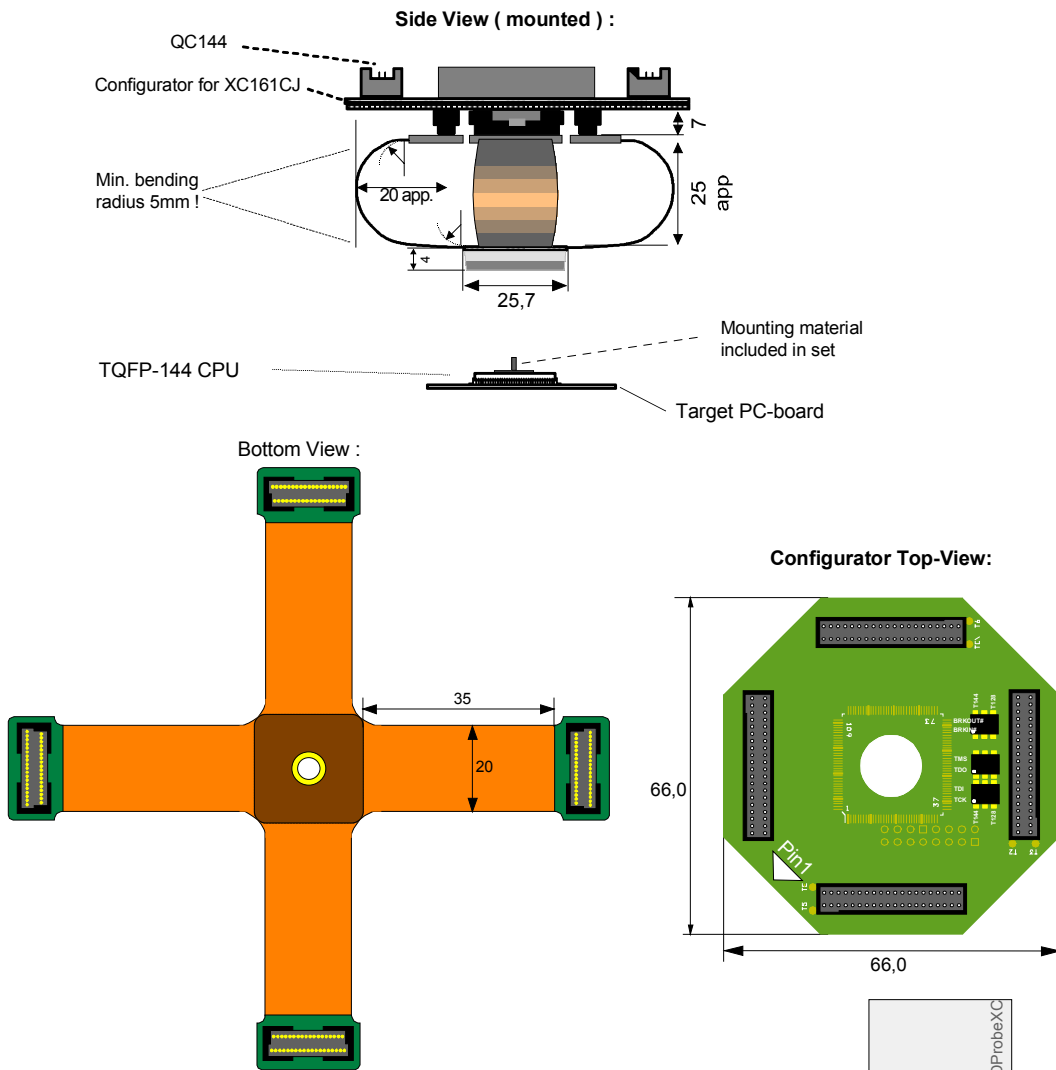


4.1.2 PressOn Adapter



**DProbeXC Adapter for Infineon XC161CJ TQFP 144 PressOn FLEX
Adapter Set DP-XC161CJ-TQFP144-PressOn
Part No. DZS-XC161-T144-P**

Top Connection : QC144 for DProbeXC
Bottom Connection : CPU Infineon XC161CJ TQFP-144 surface mounted.



Note: The target's TQFP CPU is disabled if the DProbeXC is connected to the PressOn adapter.

Datasheet DZS-XC161-T144-P

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Drawing not to scale !

Adapter Data Sheet

4.1.3 Yamaichi Adapter



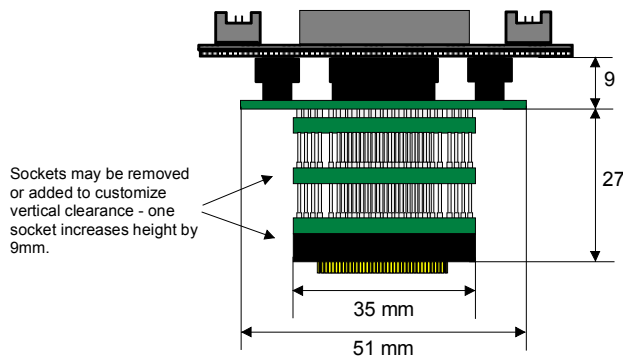
Adapter Set for XC161CJ Target Systems with TQFP-144 Yamaichi-Socket
Adapter Set QC144-TQFP144 Yamaichi-0.50 XC161CJ
Part No. DZS-XC161-T144-Y

Top Connection : QC144 for DProbeXC

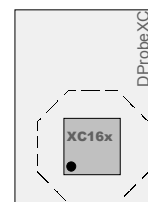
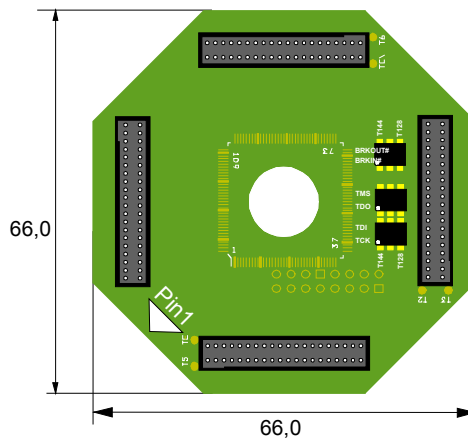
Bottom Connection : TQFP-144 Yamaichi Socket

IC 149-144-045-B5 (Recommended)
 or IC 149-144-145-B5 (Recommended)
 or IC 149-144-045-S5
 or IC 149-144-145-S5

Side view:



Configurator Top-View:



Note : For proper contact and processing the Yamaichi-Socket requires a slightly bigger footprint than the original CPU and four solder-pads at the corners of the socket as a mechanical support. (Refer to the Yamaichi-Datasheet). As a substitute for the solder-pads the socket may be stabilized with an adequate two-component glue.

Datasheet DZS-XC161-T144-Y

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Adapter Data Sheet

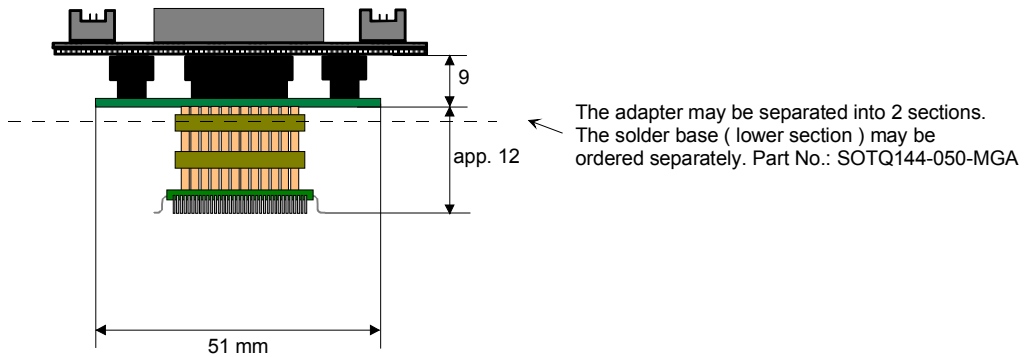
4.1.4 Replacement Adapter



Adapter Set for XC161CJ Target Systems with TQFP-144 Footprint (Solder-In)
Adapter Set QC144-TQFP144 Replacement XC161CJ
Part No. DZS-XC161-T144-REP

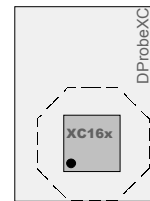
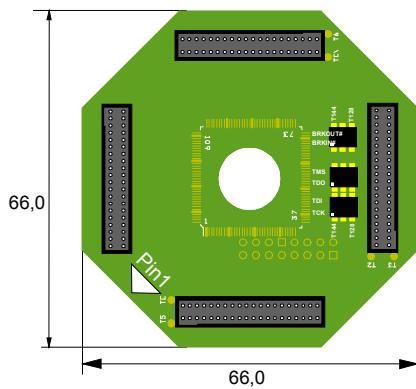
Top Connection : QC144 for DProbeXC
 Bottom Connection : TQFP-144 Footprint for Infineon XC161CJ

Side View:



Top-View :

Configurator Top-View:



Note 1: The solder base has a rotational symmetry and may be mounted in arbitrary direction using e.g. reflow equipment.

Datasheet DZS-XC161-T144-REP

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Adapter Data Sheet

4.2 Adapter Solutions for XC164CS – TQFP100

4.2.1 Quad Connector Layout



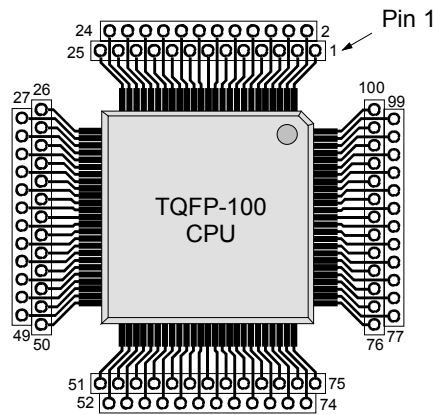
Quad Connector System QC100 25X25 Target receptacles for CPUs in P-TQFP-100-1 package

In order to use direct connection of the DProbeXC via quad connector to an XC164CS target system, four 12 pin and four 13 pin high density receptacles have to be designed around the target processor. The advantage of this adaption is a very reliable connection of the emulation system.

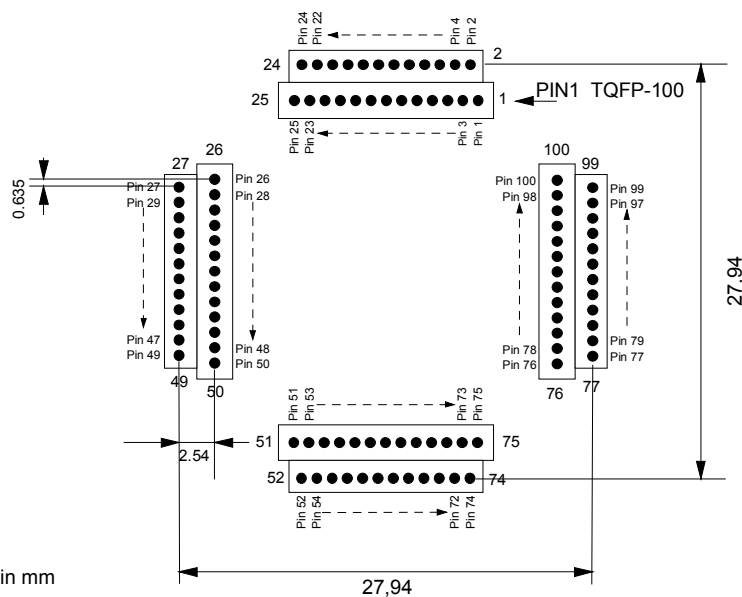
Connector-Types: SAMTEC MICRO STRIP SLM Series

Part. No.: SLM-112-01-G-S
& Part. No.: SLM-113-01-G-S

Required Target layout and connection to TQFP-100 CPU (Top view) :



Connector placement and pinout (top view)



All Dimensions in mm

February 2002

Application Note

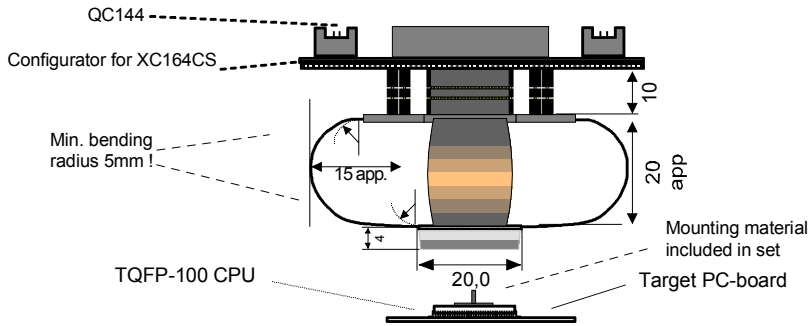
4.2.2 PressOn Adapter



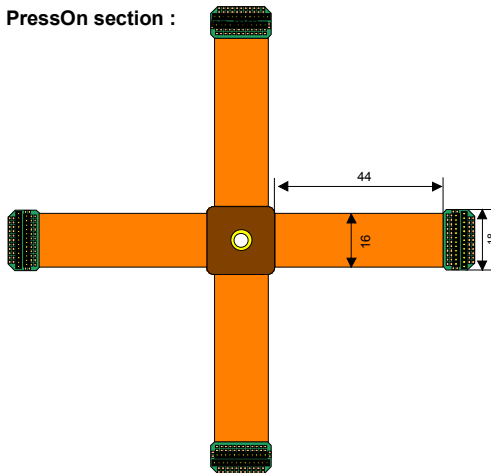
DProbeXC Adapter for Infineon XC164CS TQFP100 PressOn FLEX
 Adapter Set DP-XC164CS-TQFP100-PressOn
 Part No. DZS-XC164-T100-P

Top Connection : QC144 for DProbeXC
 Bottom Connection : CPU Infineon XC164CS TQFP-100 surface mounted.

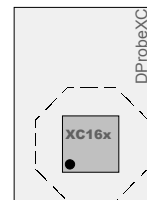
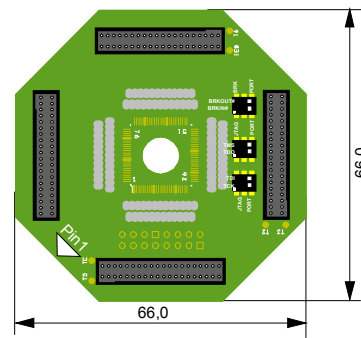
Side View (mounted) :



PressOn section :



Configurator Top-View:



Note: The target's TQFP CPU is disabled if the DProbeXC is connected to the PressOn adapter.

Datasheet DZS-XC164-T100-P

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Adapter Data Sheet

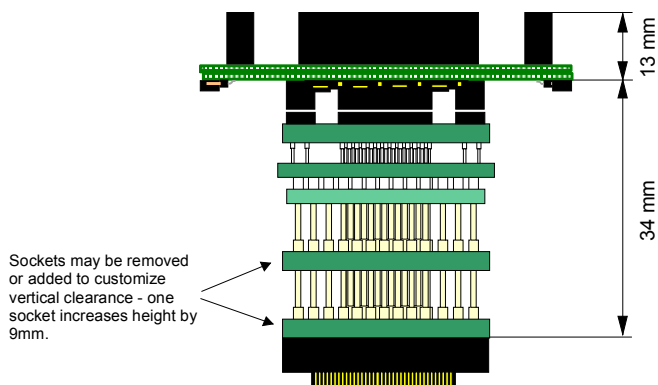
4.2.3 Yamaichi Adapter



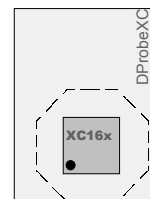
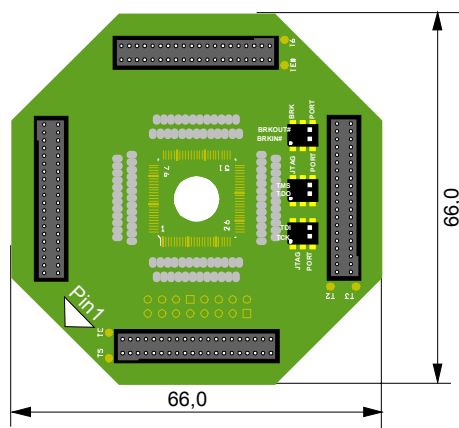
Adapter Set for XC164CS Target Systems with TQFP-100 Yamaichi Socket
 Adapter Set QC144-TQFP100 Yamaichi-0.50 XC164CS
 Part No. DZS-XC164-T100-Y

Top Connection : QC144 for DProbeXC
 Bottom Connection: TQFP100 Yamaichi Socket IC 149-100-025-B5

Side view:



Configurator Top-View:



Datasheet DZS-XC164-T100-Y

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Adapter Data Sheet

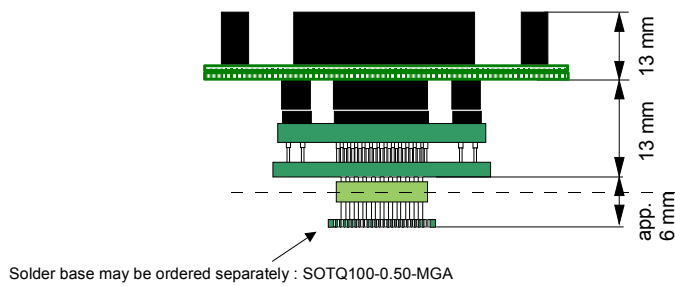
4.2.4 Replacement Adapter



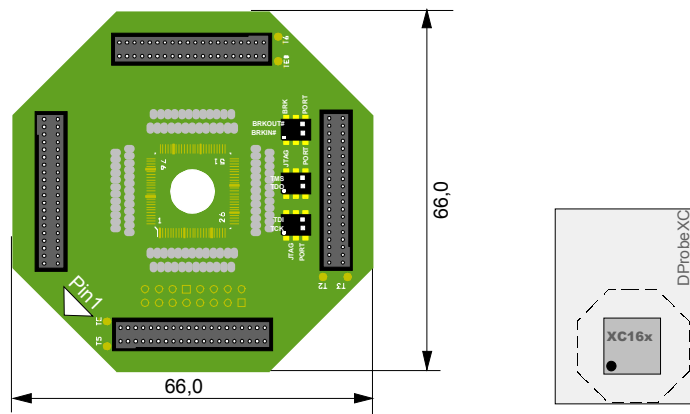
Adapter Set for XC164CS Target Systems with TQFP-100 Footprint (Solder-In)
 Adapter Set QC144-TQFP100 Replacement XC164CS
 Part No. DZS-XC164-T100-REP

Top Connection : QC144 for DProbeXC
 Bottom Connection: TQFP-100 Footprint for Infineon XC164CS

Side/Front View:



Configurator Top-View:



Note 1: The solder base has got rotational symmetry and may be soldered (e.g. by reflow) in arbitrary direction - however when installing the upper section of the adapter the "Pin-1 C161RI" mark on the adapter and the Pin-1 orientation of the target footprint have to be aligned !

Datasheet DZS-XC161-T144-REP
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Adapter Data Sheet

5. Target Design Considerations

In order to use PressOn adaptation, please make sure that the following design considerations are taken into account.

- For Single-Chip designs, the EA pin may not be connected directly to Vcc. To get the specified board setup (single-chip mode reset), the EA pin has to be pulled to Vcc via an 8k2 resistor. This allows the DProbeXC to force the soldered device into adapt-mode (tristate) and therefore allows PressOn adaptation.
- Pin 1 of port 0 (POL.1) is driven low by the emulator during target reset. Therefore, if the pin is driven from the target logic during reset, a resistor (8k2) has to be placed between the driver and the pin of the target CPU.

6. Revision History

Version	Date	Details
0.1	February 7 th , 2002	initial version / pre-release
1.0	April 9 th , 2002	first release <u>changes made:</u> <ul style="list-style-type: none">• additional adapters added• order codes corrected