

Application Note

Product	<i>Tanto TriCore</i>
Information	<i>Target Interface Description</i>
Derivative	<i>Infineon TriCore</i>
Version	<i>0.4</i>
Date	<i>26.March 2002</i>

1. Preface

This application note is an information on the necessary debug interface to be implemented on TriCore-based target systems. The information contained herein is specifically adapted to interface with one or both of the following emulation tools from Hitex:

- Tanto TriCore
- JProbe TriCore

For further information please contact the Hitex Support Group at ++49-721-9628-0 or via mail at <mailto:support@hitex.de>.

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3. Tanto Port Link for TriCore

The Tanto Port Link (TantoPL) for TriCore allows to interface to the OCDS Level 1 and OCDS Level 2 interface. The following picture shows the interfaces on the TantoPL for TriCore:

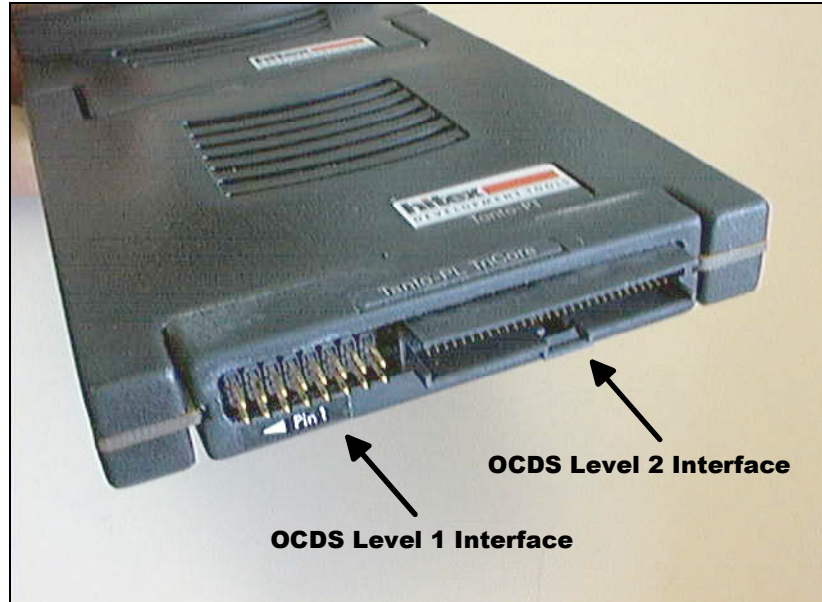


Figure 3-1: Tanto Port Link for TriCore

4. OCDS Level 1 Debug Interface

The Tanto Base system is connected to the target system via a flat ribbon cable with female plugs and is connected to male headers on the Tanto Port Link and on the target. The OCDS1 connector defined by Infineon is a 16-pin standard 0.1 inch header (2 rows, 8 pins). This connector is referred to as Connector Type A.

A 20-pin 0.05 inch SMD header (Samtec FTSH type) will also be provided by a specific cable driver to the TantoPL which requires less space. It is available with a keying shroud (FTSH-110-01-L-DV-K). This connector is referred to as Connector Type B.

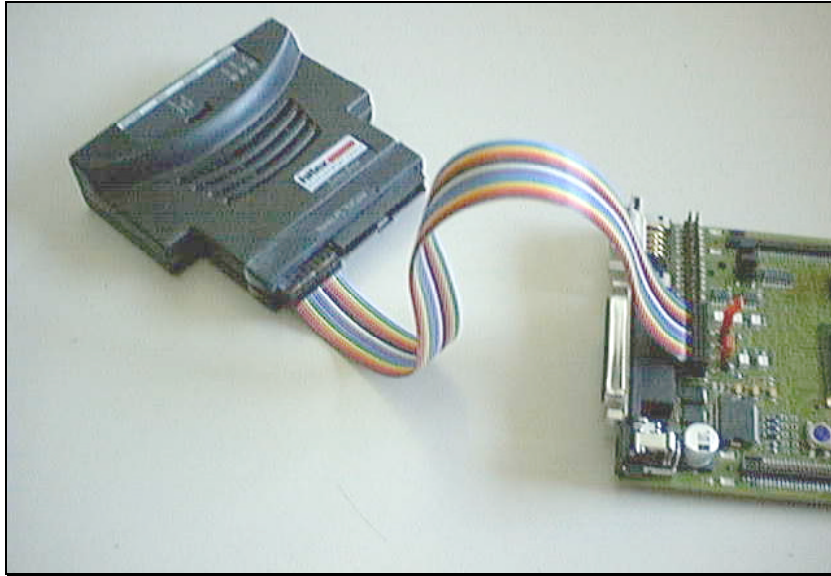


Figure 4-1: Connection of Tanto Base via OCDS Level 1 interface (Connector Type A)

Please refer to the following chapters regarding dimensions and pinout of the interface connectors.

4.1 Description of OCDS Level 1 Connector (Type A)

The following table shows the pin assignment and the signal description when using the 'Type A' interface (*Standard 0.1-Inch Header*).

Pull-Up/Down	Signal ¹	Pin	Dir ²	Dir	Pin	Signal	Pull-Up/Down
100kΩ PU	TMS	1	I	P	2	VCC	-
-	TDO	3	O	P	4	GND	-
-	CPU_CLOCK ³	5	O	P	6	GND	-
100kΩ PU	TDI	7	I	I ⁴	8	RESET#	10kΩ PU
10kΩ PD	TRST#	9	I	O	10	BRKOUT#	-
10kΩ PD	TCLK	11	I	P	12	GND	-
100kΩ PU	BRKIN#	13	I	I	14	OCDSE#	100kΩ PU
-	NC	15	-	-	16	no pin	-

Table 4-1: Signal Description of the OCDS1 Connector Type A

Note: For a detailed description and requirements of the IEEE1149.1 signals, please refer to the equivalent document from Infineon Technologies

- see also: http://www.hitex.de/pdf/ap4802b_OCDS_L1_Connector_V2.2.pdf

¹ Note: A '#' at the end of a signal name characterizes a low active signal

² Note: The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

³ Note: This signal is optional, and is not available on all CPUs. If the signal is not available, the pin should be left unconnected

⁴ Note: The signal RESET# is implemented as an open drain output and can therefore be connected directly to the CPU. The required Pull-Up resistor has to be implemented on the target hardware.

4.2 Description of OCDS Level 1 Connector (Type B)

The following table shows the pin assignment and the signal description when using the 'Type B' interface (*Samtec 0.05-Inch Header*).

Pull-Up/Down	Signal ¹	Pin	Dir ²	Dir	Pin	Signal	Pull-Up/Down
-	GND	1	P	P	2	GND	-
100kΩ PU	TMS	3	I	P	4	VCC	-
-	TDO	5	O	P	6	GND	-
-	CLKOUT ³	7	O	P	8	GND	-
100kΩ PU	TDI	9	I	I ⁴	10	RESET#	10kΩ PU
10kΩ PD	TRST#	11	I	O	12	BRKOUT#	-
10kΩ PD	TCLK	13	I	P	14	GND	-
100kΩ PU	BRKIN#	15	I	I	16	OCDSE#	100kΩ PU
-	NC	17	-	-	18	GND	-
-	GND	19	-	-	20	GND	-

Table 4-2: Signal Description of OCDS1 Connector Type B

Note: For a detailed description and requirements of the IEEE1149.1 signals, please refer to the equivalent document from Infineon Technologies

- see also: http://www.hitex.de/pdf/ap4802b_OCDS_L1_Connector_V2.2.pdf

¹ **Note:** A '#' at the end of a signal name characterizes a low active signal

² **Note:** The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

³ **Note:** This signal is optional, and is not available on all CPUs. If the signal is not available, the pin should be left unconnected

⁴ **Note:** The signal RESET# is implemented as an open drain output and can therefore be connected directly to the CPU. The required Pull-Up resistor has to be implemented on the target hardware.

5. OCDS Level 2 Debug Interface

Currently there are 2 different interfaces available:

- high speed interface
- low speed interface (< 40MHz)

The Tanto development system can be connected via specific cable drivers to both interfaces. The following figure shows the connection of the Tanto development system to the infineon evaluation board (TC1775) via OCDS Level 1 interface and OCDS Level 2 interface with the low speed cable Driver Board.

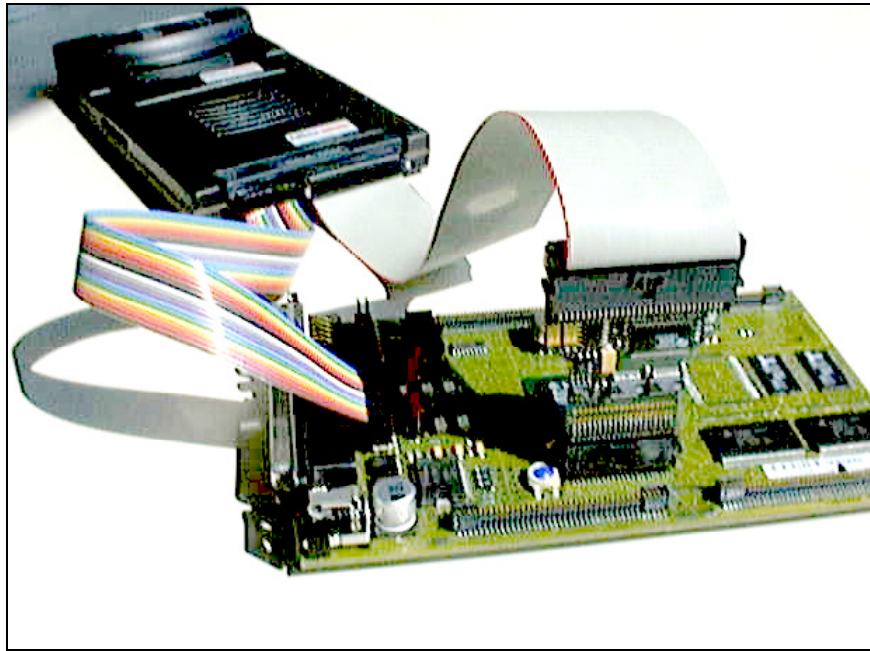


Figure 5-1: Connection of Tanto via Level 1 and Level 2 interface

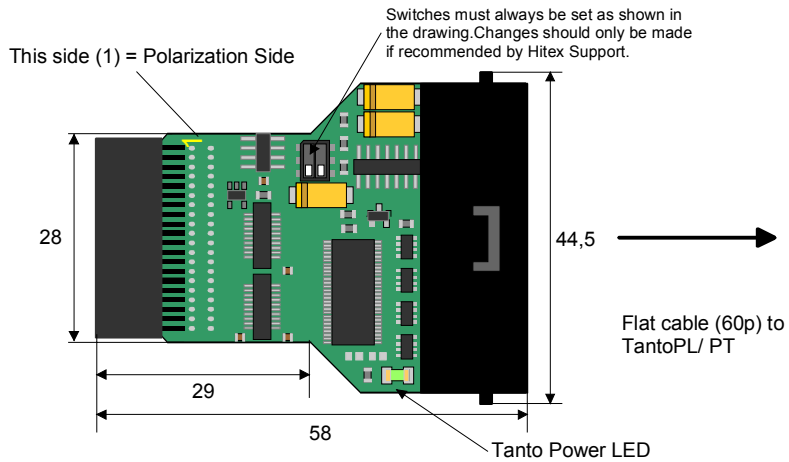
Please refer to the following chapters regarding dimensions and pinout of the interface connectors.

5.1 Low Speed Interface Cable Driver

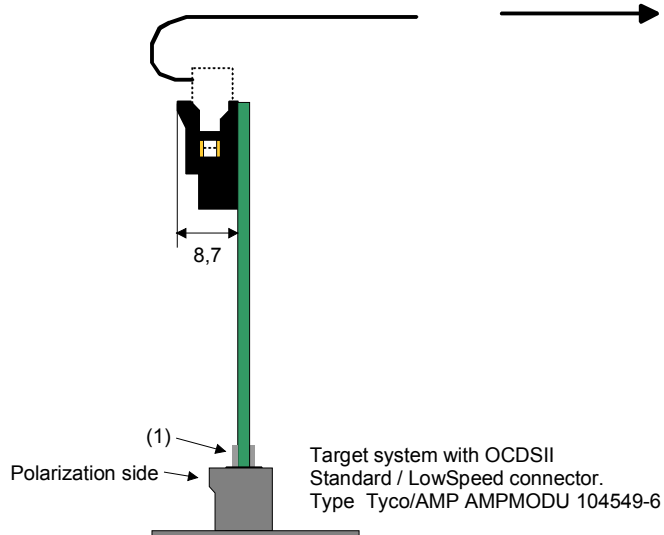


Tanto-PT Portlink Cable Driver TriCore OCDS2
 Cable Driver Type: OCDS2 - Low Speed - Vertical
 Part No. TZS-TC1-LS-V

Top view



Side view



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Data Sheet

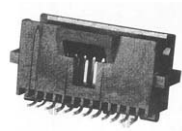
Figure 5-2: Dimension of OCDS Level 2 Low Speed Connector

5.2 Low Speed Interface Connection Diagram

Signal ¹	Pin	Dir ²		Dir	Pin	Signal
CLKOUT ³	1	O		P	2	GND
-	3			O	4	STATUS0
STATUS1	5	O		O	6	STATUS2
STATUS3	7	O		O	8	STATUS4
-	9				10	-
-	11			P	12	GND
-	13			O	14	INDPC0
INDPC1	15	O		O	16	INDPC2
INDPC3	17	O		O	18	INDPC4
INDPC5	19	O		O	20	INDPC6
INDPC7	21	O			22	-
-	23				24	-
-	25			P	26	GND
-	27			O	28	BRKPT0
BRKPT1	29	O		O	30	BRKPT2
NC ⁴	31	(O)		-	32	NC ⁵
(PCPBRKOUT#) ⁶	33	O			34	-
-	35			P	36	VCC
-	37				38	-
-	39			P	40	GND

Table 5-1: Signal Description of the OCDS Low Speed Connector

Note: Signals in brackets are only connected if supported by the respective TriCore derivative



Connector Type in Target System: AMP104549-6

For more details, please refer to the equivalent Infineon documentation.

- see also: http://www.hitex.de/pdf/ap3258b_OCDS_L2_Connector_V2.3.pdf

¹ Note: A '#' at the end of a signal name characterizes a low active signal

² Note: The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

³ Note: It is recommended to insert a series resistor between the signal CLKOUT of the TriCore derivative and the above shown OCDS Level2 interface connector. The series resistor should be in the range of 22Ω and 33Ω.

⁴ Note: Pin31 of the connector shown above is defined in the Infineon specification as the BRKOUT# signal of the CPU. This signal is used from the OCDS1 connector and therefore remains unconnected on the connector shown above.

⁵ Note: Pin32 of the above shown connector is defined in the Infineon specification as the BRKIN# signal of the CPU. This signal is used from the OCDS1 connector and therefore remains unconnected on the connector shown above. This signal will not be driven by the Hitex OCDS adapters.

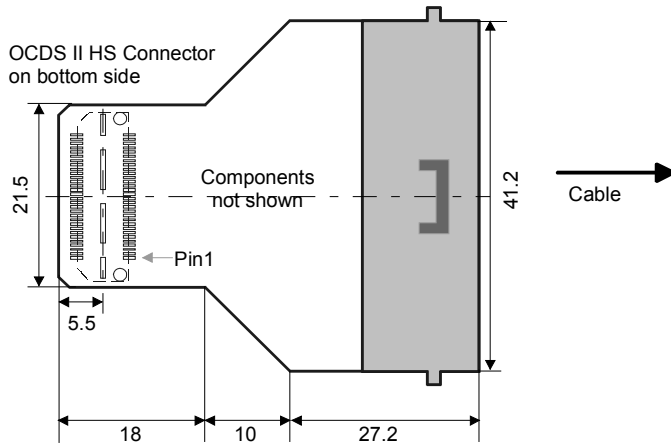
⁶ Note: If signal PCPBRKOUT# is not available the TriCore derivative, this pin should be left unconnected.

5.3 High Speed Interface Cable Driver

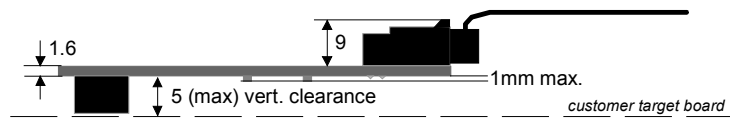


Tanto-PT Portlink Cable Driver TriCore OCDS2
 Cable Driver Type: OCDS2 - HighSpeed - Horizontal
 Part No. TZS-TC1-HS-H

Top view



Side view



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Adapter Data Sheet

Figure 5-3: Dimension of OCDS Level 2 High Speed Connector

5.4 High Speed Interface Connection Diagram

Signal ¹	Pin	Dir ²	Dir	Pin	Signal
(NC) ³	1	I	O	2	BRKPT2
-	3	I	O	4	BRKPT1
-	5	I	O	6	-
-	7	I	P	8	VCC IO RING
-	9	I	O	10	BRKPT0
-	11	I	O	12	STATUS4
-	13	I	O	14	STATUS3
-	15	I	O	16	STATUS2
-	17	I	O	18	STATUS1
-	19	O	O	20	STATUS0
-	21	O	O	22	-
-	23	O	O	24	-
-	25	P	O	26	-
-	27	O	O	28	-
(PCP PC OR) ⁴	29	I/O	O	30	-
(PCPBRKOUT#)	31	I/O	O	32	-
NC ⁵	33	I	O	34	-
* see note* NC⁶	35	O	O	36	IND PC7
-	37	I/O	O	38	IND PC6
(PCP PC8)	39	I/O	O	40	IND PC5
(PCP PC7)	41	I/O	O	42	IND PC4
(PCP PC6)	43	I/O	I/O	44	-
(PCP PC5)	45	I/O	I/O	46	-
(PCP PC4)	47	I/O	O	48	IND PC3
(PCP PC3)	49	I/O	O	50	IND PC2
-	51	I/O	O	52	IND PC1
-	53	I/O	O	54	IND PC0
(PCP PC2)	55	I/O	P	56	VCC IO RING
(PCP PC1)	57	I/O	I	58	(OCDS L2 EN) ⁴
(PCP PC0)	59	I/O	O	60	CLKOUT ⁷

Table 5-2: Signal Description of the OCDS High Speed Connector

Note: Signals in brackets are only connected if supported by the respective TriCore derivative (see also Note 4)

For more details, please refer to the equivalent Infineon documentation.

- see also: http://www.hitex.de/pdf/ap326011_OCDS_L1L2_Connector_V1.1.pdf

¹ Note: A '#' at the end of a signal name characterizes a low active signal

² Note: The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

³ Note: Pin1 of the connector shown above is defined in the Infineon specification as the POR# signal of the CPU. This signal is connected to the OCDS1 connector and therefore remains unconnected on the connector shown above. This signal will not be driven by the Hitex OCDS adapters.

⁴ Note: If the signal is not available on a TriCore derivative, the appropriate pin should be left unconnected.

⁵ Note: Pin33 of the connector shown above was previously defined as the BRKIN# signal of the CPU. This signal is used from the OCDS1 connector and remains therefore unconnected on the connector shown above. This signal will not be driven by the Hitex OCDS adapters.

⁶ Note: Pin35 of the connector shown above was previously defined as the BRKOUT# signal of the CPU. This signal is used from the OCDS1 connector and remains therefore unconnected on the connector shown above. **This pin must be left unconnected, when debugging is made via 2 separate connectors (OCDS1 and OCDS2).**

⁷ Note: It is recommended to insert a series resistor between the signal CLKOUT of the TriCore derivative and the above shown OCDS Level2 interface connector. The series resistor should be in the range of 22Ω and 33Ω.

6. Combined Connector Interface

In addition to the OCDS2 target interfaces described in chapter 5, a further variant is available, which combines the OCDS1 and OCDS2 interfaces on a single connector.

Using this interface does not require a separate OCDS1 interface connector on the target system anymore and therefore saves board space. Chapter 6.1 and chapter 6.2 describe the interface in detail.

Please note, that this interface can only be used with the latest version of the Port-Link module (TantoPL-TC) for TriCore (Revision 1.2).

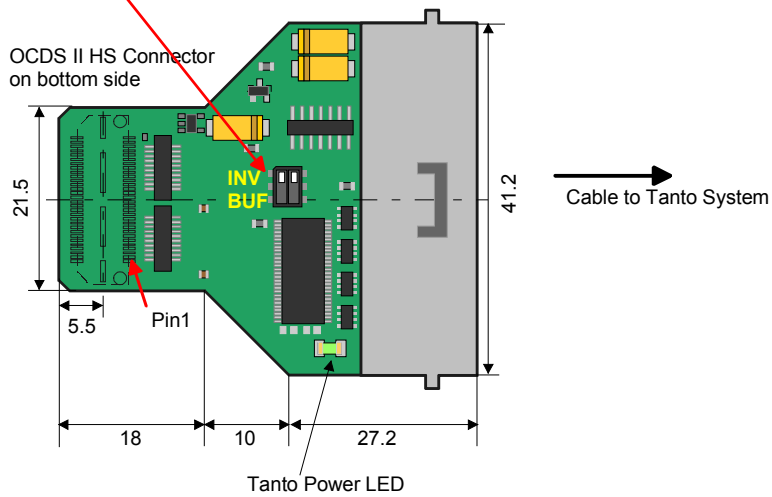
6.1 Combined Interface Cable Driver



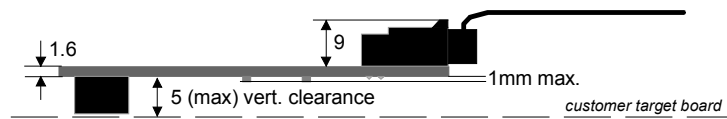
Tanto-PT Portlink Cable Driver TriCore OCDS1&2
 Cable Driver Type: OCDS2 - HighSpeed - Combined - Horizontal
 Part No. TZS-TC1-HS-C-H

Trace Data is sampled with the:
 INV: falling edge of CLKOUT(default)
 BUF: rising edge of CLKOUT

Top view



Side view



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Figure 6-1: Dimension of combined High Speed Connector

6.2 Combined Interface Connection Diagram

Pull-Up/Down	Signal ¹	Pin	Dir ²	Dir	Pin	Signal	Pull-Up/Down
10kΩ PU	RESET#	1	I ³	O	2	BRKPT2	
100kΩ PU	BRKIN#	3	I	O	4	BRKPT1	
10kΩ PD	TRST#	5	I	-	6	-	
	-	7	-	P	8	VCC IO RING	
	-	9	-	O	10	BRKPT0	
100kΩ PU	OCDSSEN#	11	I	O	12	STATUS4	
100kΩ PU	TDI	13	I	O	14	STATUS3	
10kΩ PD	TCK	15	I	O	16	STATUS2	
	-	17	-	O	18	STATUS1	
	-	19	-	O	20	STATUS0	
	-	21	-	-	22	-	
	-	23	-	-	24	-	
	-	25	-	-	26	-	
	BRKOUT#	27	O	O	28	TDO	
	(PCP PC OR) ⁴	29	O	-	30	-	
	(PCPBRKOUT#)	31	O	-	32	-	
	-	33		-	34	-	
	GND ⁵	35	I	O	36	IND PC7	
	-	37	-	O	38	IND PC6	
	(PCP PC8)	39	O	O	40	IND PC5	
	(PCP PC7)	41	O	O	42	IND PC4	
	(PCP PC6)	43	O	I	44	TMS	100kΩ PU
	(PCP PC5)	45	O	-	46	-	
	(PCP PC4)	47	O	O	48	IND PC3	
	(PCP PC3)	49	O	O	50	IND PC2	
	-	51	-	O	52	IND PC1	
	-	53	-	O	54	IND PC0	
	(PCP PC2)	55	O	P	56	VCC IO RING	
	(PCP PC1)	57	O	I	58	(OCDS L2 EN#) ⁴	100kΩ PU
	(PCP PC0)	59	O	O	60	CLKOUT ⁶	

Table 6-1: Signal Description of the OCDS High Speed Connector (combined version)

Note: Signals in brackets are only connected if supported by the respective TriCore derivative
A '-' (dash) in the signal column, refers to a n.c. pin

Important Note on Pin 35

This pin is used by the emulator hardware to detect whether the OCDS1 interface signals are used from a separate OCDS1 connector or from the above shown combined connector. If the target hardware does not apply a GND-level to this pin, the standard high speed cable driver must be used (refer to chapter 5.3 and 5.4).

For more details, please refer to the equivalent Infineon documentation.

- see also: http://www.hitex.de/pdf/ap326011_OCDS_L1L2_Connector_V1.1.pdf

¹ Note: A '#' at the end of a signal name characterizes a low active signal

² Note: The direction shown in the above table is referred to the CPU

- 'I' = Input of the CPU
- 'O' = Output of the CPU
- 'P' = Power Signal of the CPU

³ Note: The signal RESET# is implemented as an open collector output and can therefore be connected directly to the CPU. The required Pull-Up resistor has to be implemented on the target hardware.

⁴ Note: If the signal is not available on a TriCore derivative, the appropriate pin should be left unconnected.

⁵ Note: Pin35 of the connector shown above must be connected to GND, to order to use the combined features of this connector. If this signal is left unconnected, a second OCDS Level 1 connector must be used for debugging.

⁶ Note: It is recommended to insert a series resistor between the signal CLKOUT of the TriCore derivative and the above shown OCDS Level2 interface connector. The series resistor should be in the range of 22Ω and 33Ω.

7. Revision History

Version	Date	Details
0.1	August 24 th , 2001	initial version – preliminary
0.2	November 20 th , 2001	Notes on Pin assignments for Level 2 Connectors added
0.3	March 6 th , 2002	Combined Connector Interface added
0.4	March 25 th , 2002	<ul style="list-style-type: none">• Tables redone• PullUp values added• Combined interface corrected• Order Codes corrected