

Philips 80C51MX

DProbeHS fully supports the Philips 80C51MX Memory eXtension

Philips Semiconductors has extended its 80C51 architecture to support up to 16 MB of Program and Data Memory.

The 80C51MX retains 100% code compatibility with the 80C51 instruction set. Due to the increased on-chip functionality and performance enhancements, design engineers can develop more sophisticated applications at a lower cost.

Engineers already comfortable with the 80C51 are now free to develop new more complex applications without having to switch to a new unfamiliar processor architecture, thereby minimizing their time to market.

The increased program memory enables 80C51MX applications to be developed in a high-level language such

as C without struggling to contain the program in the traditional 64 KB of program memory. The enhancements also improve C language efficiency for code size below 64 KB.

The 80C51MX also retains compatibility with the original 80C51 bus, allowing re-use of 80C51-interfaced peripherals and ASICs.

This advancement lays down a future migration path for developers to progress beyond the current 64 KB barrier imposed by the industry standard 80C51 architecture.

The DProbeHS In-Circuit Emulator from Hitex fully supports the 80C51MX and all of its enhancements.

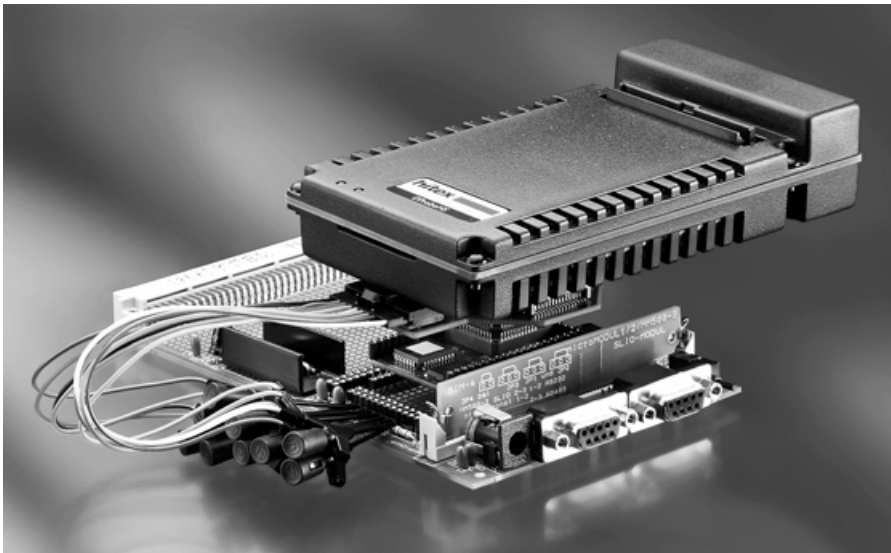
Highlights

DProbeHS for the 80C51MX

- Small high-end real-time in-circuit emulator, non-intrusive
- Support of all 80C51MX specific enhancements
- Supports highest speed (up to 70 MHz)
- Modular system, no overhead
- Easy emulation processor setup
- Interrupt support while emulation is halted
- Watchdog support
- 1 MB dual-ported emulation memory, on-the-fly access to variables, shadow RAM functionality for external data
- 1M hardware breakpoints for code, data read and data write
- RIAS™ (with DBox16)
- Macro language HiSCRIPT
- Support for all popular compilers

DProbeHS with DBox16

- Intelligent real-time trace with 32...256K frames, 96 bit, update on-the-fly, filter feature (address, data, status, external inputs, time stamp)
- 4 complex triggers, 2...4 level sequence
- Timer trigger feature
- Code coverage
- Protection
- Read-before-written detection
- Performance analysis



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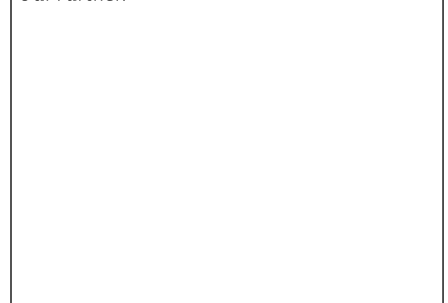
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